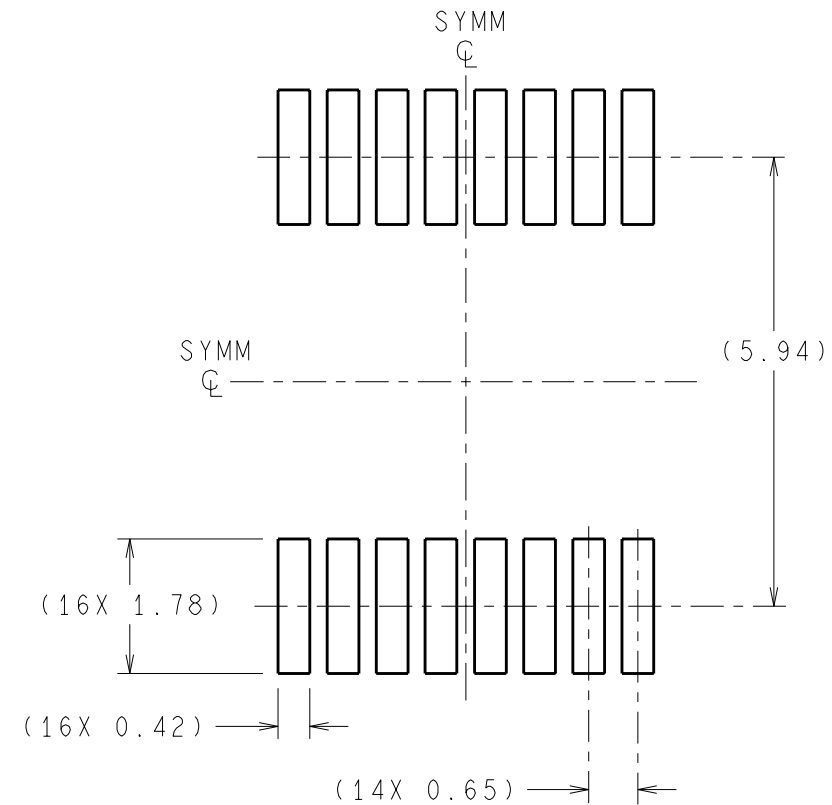
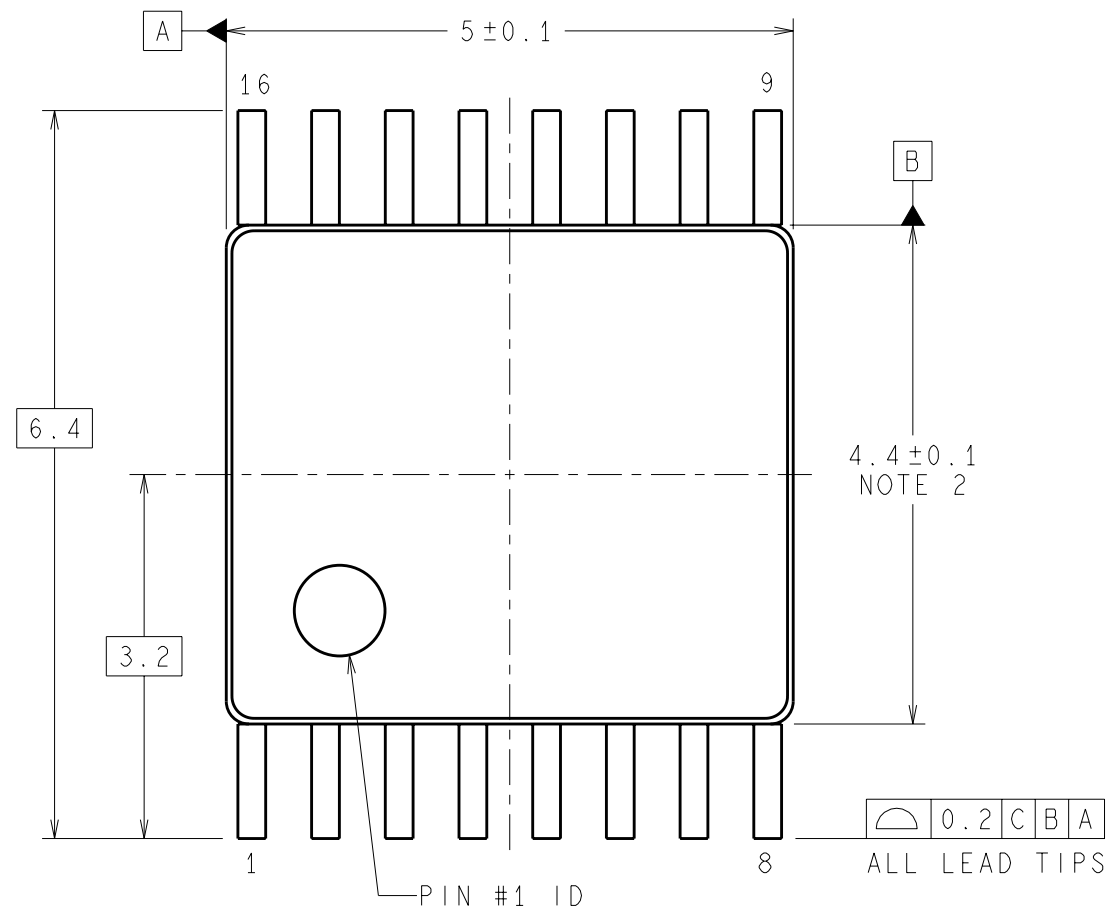
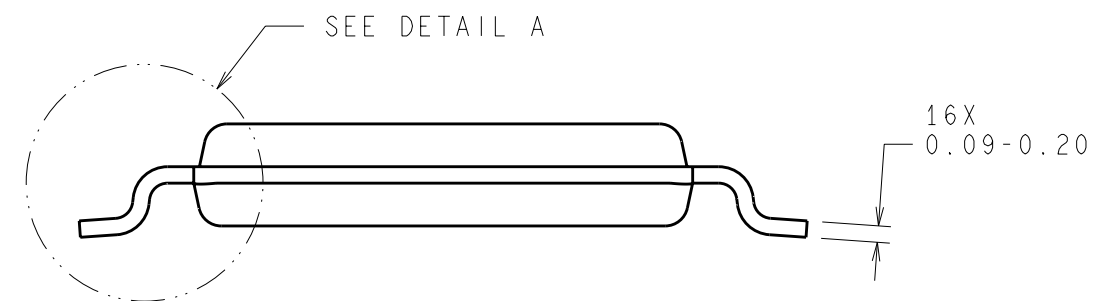
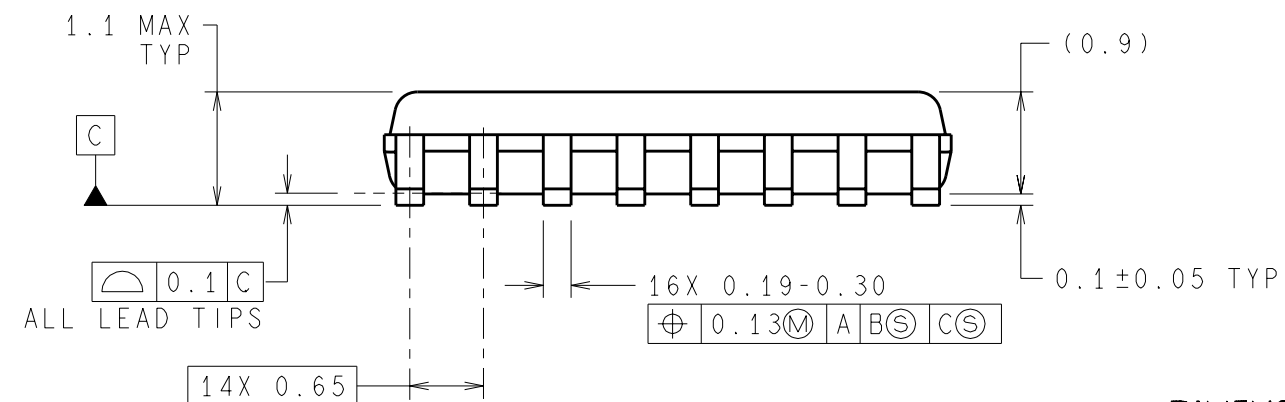


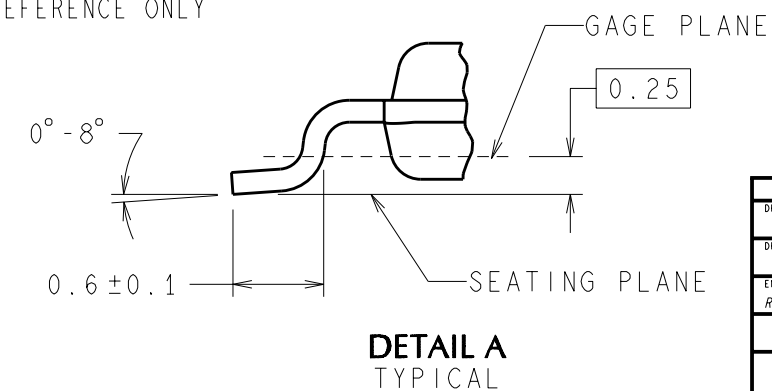
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
C	REVISE & REDRAW ON PROVE PER CURRENT STD; CORRECT DET CALLOUT FROM D TO A	11104	08/29/1995	MS/TC
D	REVISE PER CURRENT STD; ADD SOLDER & MOLD FLASH NOTES; UPDATE TITLE; CHG DWG FORMAT TO B SIZE	1043	06/10/2003	TL/RW



RECOMMENDED LAND PATTERN



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY



NOTES: UNLESS OTHERWISE SPECIFIED

- FOR LEAD FINISH THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
- DIMENSION DOES NOT INCLUDE MOLD FLASH.
- REFERENCE JEDEC REGISTRATION MO-153, VARIATION AB.

APPROVALS		DATE	 National Semiconductor 2900 Semiconductor Dr., Santa Clara, CA 95052-8090	
DRAWN	MARTA SUCHY	08/29/1995		
DFTG. CHK.	MARTA SUCHY	06/10/2003	MOLDED TSSOP, JEDEC, 5x4.4x0.9mm BODY, 16 LD, 0.65mm PITCH	
ENGR. CHK.	RANDALL WALBERG	06/10/2003		
PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
MM	NTS	B	(SC)MKT-MTC16	D
FORMERLY: N/A			SHEET 1 of 1	